



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,957	11/02/2001	Andres Bryant	BUR920010071US1	3893

23123 7590 05/14/2003
SCHMEISER OLSEN & WATTS
18 E UNIVERSITY DRIVE
SUITE # 101
MESA, AZ 85201

EXAMINER

LEWIS, MONICA

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 05/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/682,957

Applicant(s)

BRYANT ET AL.

Examiner

Monica Lewis

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 March 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the amendment filed March 3, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 8-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (U.S. Patent No. 5,994,747) in view of Houston (U.S. Patent No. 6,045,625).

In regards to claim 8, Wu et al. ("Wu") discloses the following:

- a) a semiconductor wafer overlying a semiconductor layer (2) (For Example: See Figure 9);
- b) a first recess and a second recess formed through the semiconductor layer (For Example: See Figure 9);
- c) a body (6) formed from the semiconductor layer situated between the first recess and the second recess, the body comprising a top body surface and a bottom body surface that defines a body thickness (For Example: See Figure 9);
- d) a source structure (14) formed into the first recess, the source structure comprising a source region (For Example: See Figure 9);
- e) a drain region formed into the second recess, the drain structure comprising a drain region (For Example: See Figure 9); and
- f) a top portion of the source structure and a top portion of the drain structure are within and abut the body thickness (For Example: See Figure 9).

In regards to claim 8, Wu fails to disclose the following:

- a) a semiconductor layer overlying a buried insulator having at least two layers.

Art Unit: 2822

However, Houston discloses a semiconductor with an insulation layer that has various layers (For Example: See Figure 5e). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wu to include an insulation layer that has various layers as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62).

In regards to claim 9, Wu discloses the following:

- a) a semiconductor layer (For Example: See Figure 9).

In regards to claim 9, Wu fails to disclose the following:

- a) the first layer of the buried insulator.

However, Houston discloses a semiconductor with an insulation layer (For Example: See Figure 5e). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wu to include an insulation layer as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62).

In regards to claim 10, Wu discloses the following:

- a) a semiconductor layer comprises single crystal silicon (For Example: See Column 3 Line 43).

In regards to claim 11, Wu fails to disclose the following:

- a) the buried insulator comprises three layers, wherein a second layer is different from the first layer and a third layer.

However, Houston discloses a semiconductor with an insulation layer that has various layers (For Example: See Column 2 Lines 43-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device

Art Unit: 2822

of Wu to include an insulation layer that has various layers as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62).

In regards to claim 12, Wu fails to disclose the following:

a) the first layer comprises silicon dioxide, wherein the second layer comprises silicon nitride, wherein the third layer comprises silicon dioxide.

However, Houston discloses a semiconductor with insulation layers that has silicon dioxide and silicon nitride (For Example: See Column 2 Lines 43-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wu to include an insulation layer that has silicon dioxide and silicon nitride as disclosed in Houston because it aids in providing low capacitance (For Example: See Column 2 Lines 43-60).

In regards to claim 13, Wu discloses the following:

a) a first recess and a second recess (For Example: See Figure 9).

In regards to claim 13, Wu fails to disclose the following:

a) a buried insulator.

However, Houston discloses a semiconductor with an insulation layer that has various layers (For Example: See Figure 5e). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wu to include an insulation layer that has various layers as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62).

Art Unit: 2822

In regards to claim 14, Wu discloses the following:

a) the body comprises a fin structure that comprises a top fin structure surface a bottom fin structure surface that define a fin structure thickness, wherein the top portion of the source structure and the top portion of the drain structure are below said top fin structure, and wherein said source structure and said drain structure abut the fin structure (For Example: See Figure 9).

In regards to claim 15, Wu discloses the following:

a) a silicon layer (For Example: See Figure 9);

b) a first recess and a second recess formed through the semiconductor layer (For Example: See Figure 9); and

c) a body formed from the semiconductor layer situated between the first recess and the second recess, the body comprising a top body surface and a bottom body surface that defines a body thickness (For Example: See Figure 9).

In regards to claim 15, Wu fails to disclose the following:

a) a silicon layer overlying on a buried insulator that comprises a first buried insulator on a second buried insulator different from the first buried insulator layer, wherein the first buried insulator layer is at least as thick as the silicon.

However, Houston discloses a semiconductor with an insulation layer that has various layers (For Example: See Figure 5e and Column 2 Lines 43-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wu to include an insulation layer that has various layers as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62).

In regards to claim 16, Wu fails to disclose the following:

a) the first buried insulator layer comprises silicon dioxide.

However, Houston discloses a semiconductor with an insulation layer that has silicon dioxide (For Example: See Column 2 Lines 43-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device

Art Unit: 2822

of Wu to include an insulation layer that has silicon dioxide as disclosed in Houston because it aids in providing low capacitance (For Example: See Column 2 Lines 43-60).

In regards to claim 17, Wu fails to disclose the following:

- a) the second buried insulator layer comprises silicon nitride.

However, Houston discloses a semiconductor with an insulation layer that has silicon nitride (For Example: See Column 2 Lines 43-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wu to include an insulation layer that has silicon nitride as disclosed in Houston because it aids in providing low capacitance (For Example: See Column 2 Lines 43-60).

In regards to claim 18, Wu discloses the following:

- a) a transistor (For Example: See Figure 9).

In regards to claim 19, Wu discloses the following:

- a) the transistor comprises a source structure and a drain structure in said first recess and said second recess (For Example: See Figure 9).

In regards to claim 20, Wu discloses the following:

- a) the transistor further comprises a fin structure (For Example: See Figure 9).

Response to Arguments

4. Applicant's arguments filed March 3, 2003 have been fully considered but they are not persuasive. Applicant argues that "no buried insulator (let alone two buried insulators as recited); and there is not recess that extends through the semiconductor layer." However, Houston discloses an insulation layer that has various layers (For Example: See Figure 5e). Houston discloses a crosshatch configuration that has continuous FET's. Therefore, Wu et al. ("Wu") and

Houston read on the claimed invention. Finally, Wu does disclose a recess "formed through the semiconductor layer" as claimed (For Example: See Figure 9).

Therefore, Applicant's arguments are not deemed persuasive.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

Art Unit: 2822

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

May 8, 2003



AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800